Getting to Know Vivado

Course Workbook
Table of Contents

About this Workbook  Slide 3
Pre-Lab: Workshop Pre-requisites  Slide 4
Lab 1: Understanding Vivado  Slide 7
About this Workbook

This workbook is designed to be used in conjunction with the Getting to Know Vivado course.

The contents of this workbook are created by Adiuvo Engineering & Training, Ltd.

If you have any questions about the contents, or need assistance, please contact Adam Taylor at adam@adiuvoengineering.com.
Pre-Lab
Workshop Pre-requisites
Required Hardware

There is no required hardware for this course.
Downloads and Installations

Step 1 – Download and install the following at least one day prior to the workshop. This may take a significant amount of time and drive space.

<table>
<thead>
<tr>
<th>Software</th>
<th>Download</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vivado 2020.1</td>
<td>Download</td>
</tr>
<tr>
<td>Source Project Files</td>
<td>Download</td>
</tr>
</tbody>
</table>
Lab 1
Overview and Introduction to Vivado
Lab 1: Overview and Introduction to Vivado

Step 1 – Open Vivado 2020.1.
Lab 1: Overview and Introduction to Vivado

Step 2 – Click on Create Project – This will open the New Project Wizard – Click Next.
Step 3 – Enter the project name of “01_Vivado” and select the location you want to save the project.
Lab 1: Overview and Introduction to Vivado

Step 4 – Select RTL Project.
Lab 1: Overview and Introduction to Vivado

**Step 5** – Click **ADD FILES** and select the two files downloaded from Github. For the file `average_tb.vhd`, change the HDL source to **Simulation Only**.
Lab 1: Overview and Introduction to Vivado

Step 6 – At this time we do not want to add any constraints files. Click Next.
Step 7 – Select the **ZedBoard** and click **Next**.
Lab 1: Overview and Introduction to Vivado

Step 8 – On the project summary tab, select Finish.
Lab 1: Overview and Introduction to Vivado

Step 9 – This will open Vivado in the project manager view.
Lab 1: Overview and Introduction to Vivado

Step 10 – Expand the Simulation Sources.
Step 11 – This will show the test bench and the design source to be simulated.
Lab 1: Overview and Introduction to Vivado

Step 12 – Double clicking on the VHDL files will open the source for inspection.
Lab 1: Overview and Introduction to Vivado

Step 13 – To run a simulation, click on **Run Simulation** and select **Run Behavioral Simulation**.
Lab 1: Overview and Introduction to Vivado

Step 14 – This will open the behavioral simulation view. Note the scope and objects.
Lab 1: Overview and Introduction to Vivado

Step 15 – Click on the **Untitled** tab to see the waveform of the simulation. Note this view shows the signals defined within the test bench only, not the Unit Under Test.
Step 16 – At the moment, the results are in hexadecimal but they make more sense in decimal. Select all the signals, right click, and select unsigned decimal from the radix.
Lab 1: Overview and Introduction to Vivado

Step 17 – This will change the results to decimal. Correct operation has result showing 118 then 96. This is the block average of 16 input values.
Step 18 – Often we want to be able to see the signals in the UUT. To do this, first let’s insert a divider. Right click on the **bottom signal** and select **New Divider**.
Lab 1: Overview and Introduction to Vivado

Step 19 – When prompted, enter the name **UUT** and you will see the new divider in the waveform.
Lab 1: Overview and Introduction to Vivado

Step 20 – To add in the UUT, right click on the UUT under the scope and select Add to Wave Window.
Step 21 – This will add in the UUT signals, however, some information may be missing as it was not saved during the simulation.
Step 22 – To add in the missing waveform, we need to restart the simulation. Select **Restart** from menu bar.
Step 23 – This will clear all waveform data and restart the simulation.
Lab 1: Overview and Introduction to Vivado

Step 24 – To rerun the simulation, select the **Run button** on the menu. The simulation will stop automatically.
Lab 1: Overview and Introduction to Vivado

Step 25 – When the simulation completes, you will see the highlighted line in the test bench.
Lab 1: Overview and Introduction to Vivado

Step 26 – Selecting the waveform tab again will show all the signals for the UUT.
Step 27 – If you make changes to the source code, you need to relaunch the simulation. This can be achieved using the relaunch button on the menu.
Lab 1: Overview and Introduction to Vivado

Step 28 – With the simulation complete, we are now ready to implement the design. Close the simulation view.
Lab 1: Overview and Introduction to Vivado

Step 29 – When asked to confirm, click **OK**. If a save waveform dialog pops up, select **Discard**.

![Confirm Close](image1)

![Save Waveform Configuration](image2)
Lab 1: Overview and Introduction to Vivado

Step 30 – To synthesize the design, click the green run arrow and select Run Synthesis.
Step 31 – On the Launch Runs dialog, select the number of jobs you want to run on your system and click OK.
Step 32 – When synthesis is complete, you will see a dialog box appear.
Step 33 – Select Open Synthesized Design.
Step 34 – This will open the synthesis view. From the menu layout, select I/O Planning.
Step 35 – Expand the **Data_In, Result and Scalar Ports** and assign them to pins. All EXCEPT the clock pin can be assigned to any pin.
Lab 1: Overview and Introduction to Vivado

Step 36 – Assign the **clock pin to Y9**. Clocks have to be assigned to clock capable pins.
Lab 1: Overview and Introduction to Vivado

Step 37 – Ensure the **IO Standard** is set to **LVCMOS18**. Do not leave it as default because this will lead to a failure to implement and generate a bitstream.
Lab 1: Overview and Introduction to Vivado

Step 38 – Save the **Constraints** we just edited.
Lab 1: Overview and Introduction to Vivado

Step 39 – This will present two new dialogs. Click **OK** on the first and enter a **file name** for the second.
Lab 1: Overview and Introduction to Vivado

Step 40 – Close the Synthesis View.
Step 41 – Confirm the decision to close by clicking **OK**. This will take us back to the project manager view.
Lab 1: Overview and Introduction to Vivado

Step 42 – We are now ready to Run Implementation.
Lab 1: Overview and Introduction to Vivado

**Step 43** – Click **Yes** when the Synthesis Out-of-Date dialog pops up.
Lab 1: Overview and Introduction to Vivado

Step 44 – Select OK on the Lunch Runs dialog.
Lab 1: Overview and Introduction to Vivado

Step 45 – When the implementation completes, you will see a dialog appear. Select **Generate Bitstream**.
Lab 1: Overview and Introduction to Vivado

Step 46 – A dialog box will appear when the bitstream generates. Congratulations you have completed your first Vivado FPGA implementation.