Setting Up the Design Rules

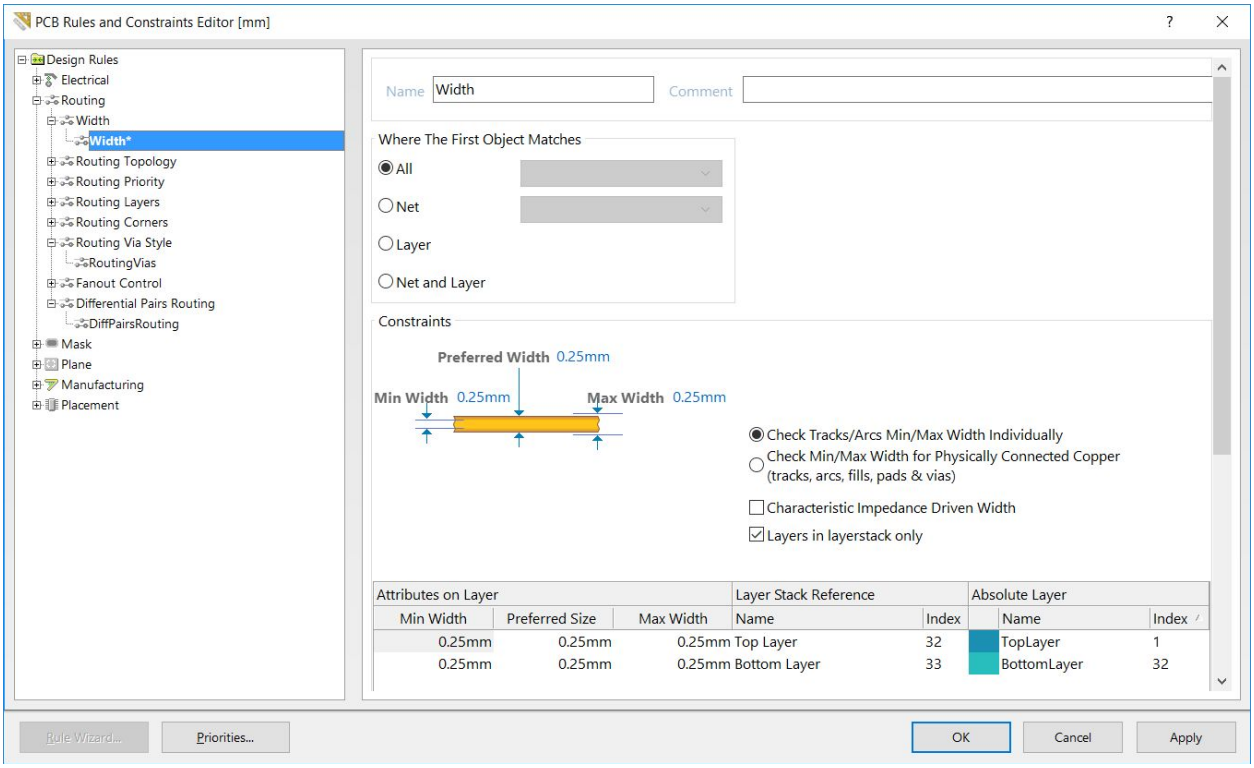
The PCB Editor is a rules-driven environment, meaning that as you perform actions that change the design, such as placing tracks, moving components, or autorouting the board, the software monitors each action and checks to see if the design still complies with the design rules. If it does not, then the error is immediately highlighted as a violation. Setting up the design rules before you start working on the board allows you to remain focused on the task of designing, confident in the knowledge that any design errors will immediately be flagged for your attention.

Design rules are configured in the *PCB Rules and Constraints Editor* dialog (**Home Tab → Design Rules | Design Rules**). The rules fall into 6 categories, which can then be further divided into design rule types. The rules cover electrical, routing, mask, plane, manufacturing and placement requirements.

Configuring the Routing Width Rule for the signal nets:

Exercise

1. With the PCB as the active document, open the *PCB Rules and Constraints Editor*.
2. Each rule category is displayed under the **Design Rules** folder (left hand side) of the dialog. Double-click on the **Routing** category to expand the category and see the related routing rules. Then double-click on **Width** to display the currently defined width rules.
3. Click once on the existing Width rule to select it. When you click on the rule, the right hand side of the dialog displays the settings for that rule, including: the rule's **Where the First Object Matches** (also referred to as the rule's *scope* - what you want this rule to target) in the top section; with the rule's **Constraints** below that.

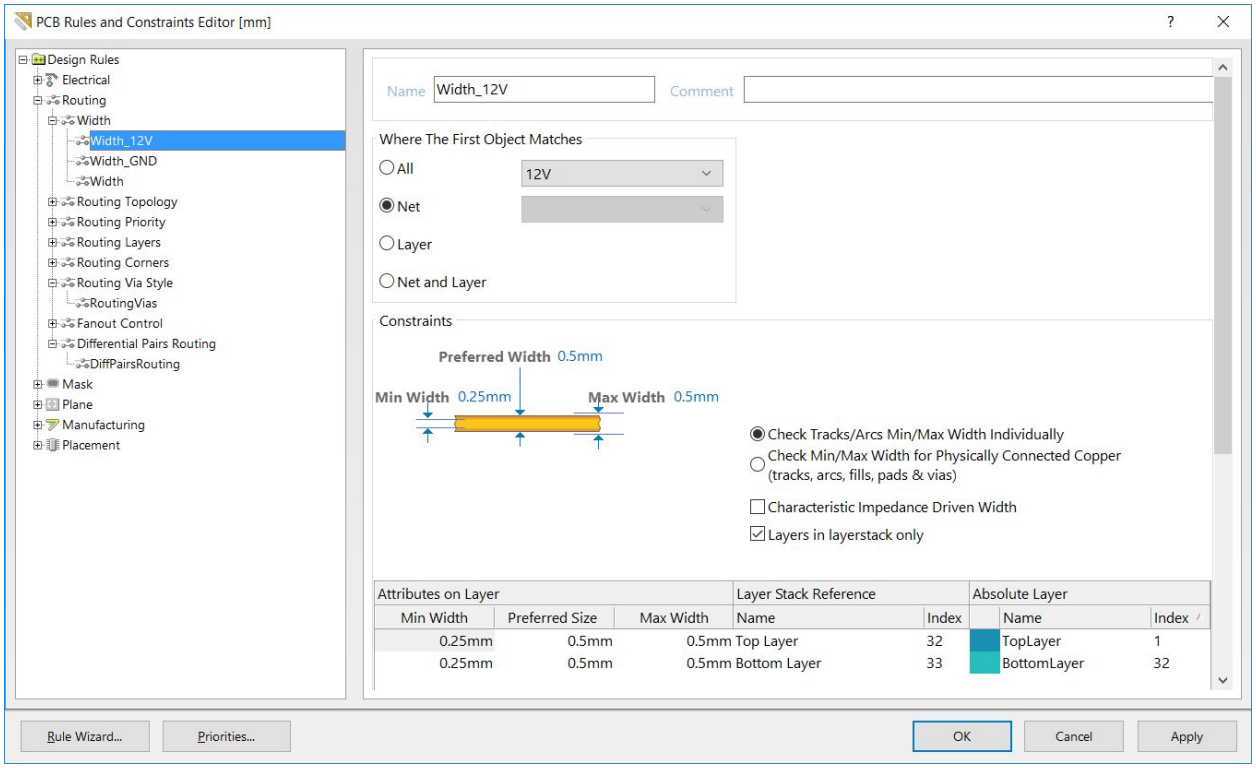


4. Since this rule is to target the majority of nets in the design (the signal nets), confirm that the **Where the First Object Matches** setting is set to All.
5. The settings in this rule are the defaults for a new PCB, edit the **Min Width**, **Preferred Width** & **Max Width** values, setting them to 0.25mm. Note that the settings are reflected in the individual layers shown at the bottom of the dialog, you can also configure the requirements on a per-layer basis.
6. The rule is now defined, click **Apply** to save it and keep the dialog open.

Adding Routing Width Rules for the power nets:

7. The next step is to add and configure 2 new design rules to specify the routing width for the power nets. To add and configure these rules, open the *PCB Rules and Constraints Editor*.
8. With the existing Width rule selected in the Design Rules tree on the left of the dialog, right-click and select **New Rule** to add a new Width constraint rule.
9. A new rule named Width_1 appears. Click on the new rule in the Design Rules tree to configure its properties.
10. Click in the **Name** field on the right, and enter the name Width_12V in the field.
11. In the **Where the First Object Matches** setting, select **Net**, then choose the 12V net in the dropdown, as shown below.
12. The last step is to set the Constraints for the rule. Edit the **Min Width** / **Preferred Width** / **Max Width** values 0.25 / 0.5 / 0.5 to allow power net routing widths in the range 0.25mm to 0.5mm, as shown below.

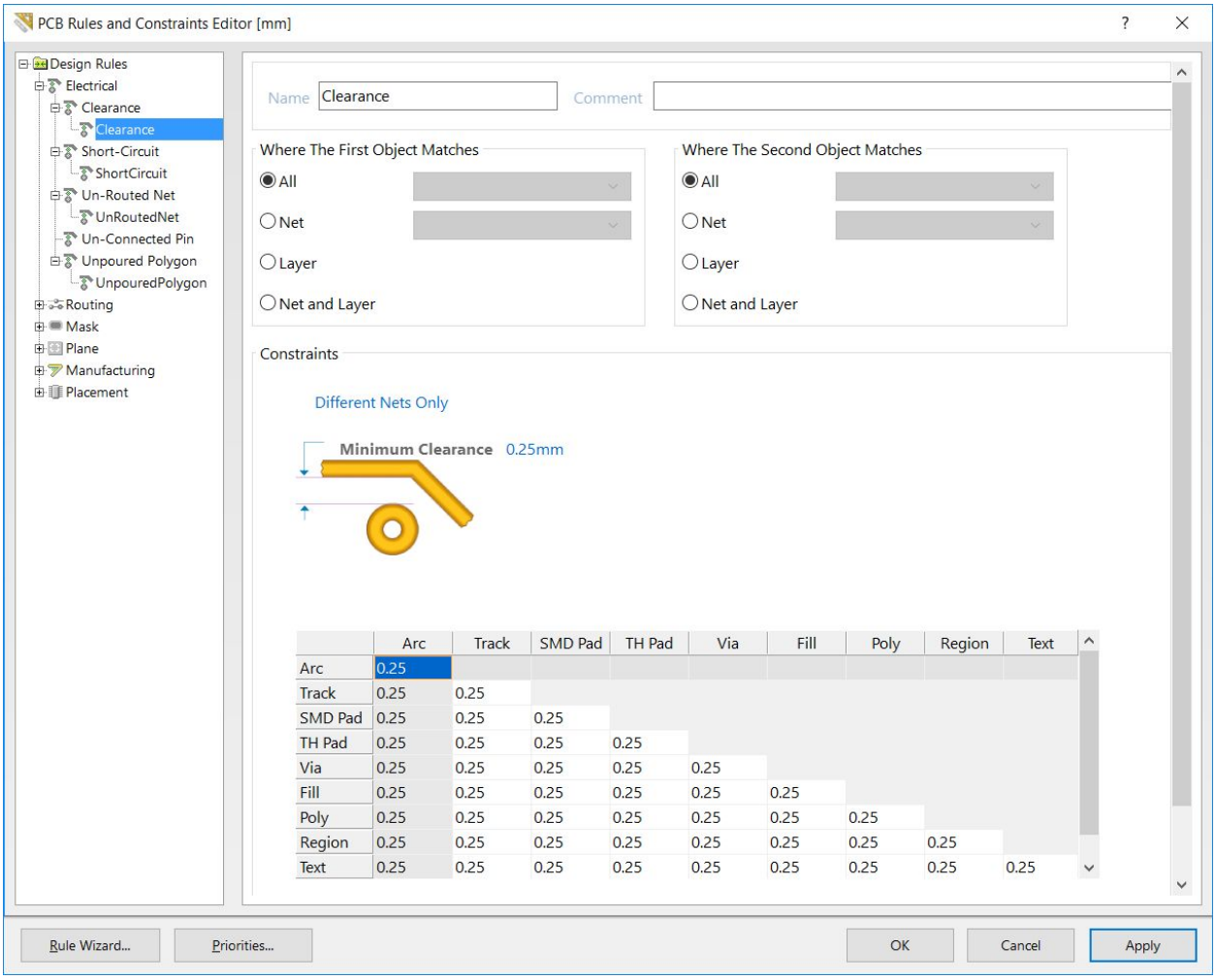
13. Repeat this sequence of steps to define another Routing Width Design Rule that targets the GND net, with the same **Constraints** values. The easiest way to do this is to use the **Duplicate Rule** command in the right-click menu, then change the **Name** of this new rule to Width_GND, and the **Net** to GND.
14. Click **Apply** to save the rules and keep the dialog open.



Defining the Electrical Clearance Constraint:

Exercise

1. Expand the Electrical category in the tree of Design Rules, then expand the Clearance rule-type.
2. Click to select the existing Clearance constraint. Note that this rule has two scope fields, that is because it is a *Binary rule*. The rules engine checks each object targeted by the setting **Where the First Object Matches** and checks it against the objects targeted by the **Where the Second Object Matches** setting, to confirm that they satisfy the specified **Constraints** settings. For this design, it is suitable to define a single clearance between All objects.
3. In the **Constraints** region of the dialog, set the **Minimum Clearance** to 0.25mm.
4. Click **Apply** to save the rule and keep the dialog open.



Defining the Routing Via Style Design Rule:

Exercise

1. Expand the Design Rule tree and select the default RoutingVias design rule.
2. Since it is highly likely that the power nets can be routed on a single side of the board, it is not necessary to define a routing via style rule for signal nets and another routing via style rule for power nets. Edit the rule settings to the values suggested earlier in the tutorial, that is a **Via Diameter** = 1mm and a **Via Hole Size** = 0.6mm. Set all fields (Min, Max, Preferred) to the same size. Note that you can press **Tab** on the keyboard to move from one dialog field to the next.

3. Click **OK** to close the *PCB Rules and Constraints Editor*.
4. **File → Save All**.

Existing Design Rule Violation

You might have noticed that the transistor pads are showing that there is a violation. Right-click over a violation and select the **Violations** in the right-click menu, as shown below. The details show that there is a:

- Clearance Constraint violation
- Between a Pad on the MultiLayer, and a Pad on the MultiLayer
- Where the clearance is 0.22mm, which is less than the specified 0.25mm

Don't worry about this violation for now, we will resolve it a bit later.

OK, that should have us set up well, and with our documents all saved, we are ready to get our PCB Placed and Routed, then we can set up and generate our outputs.
