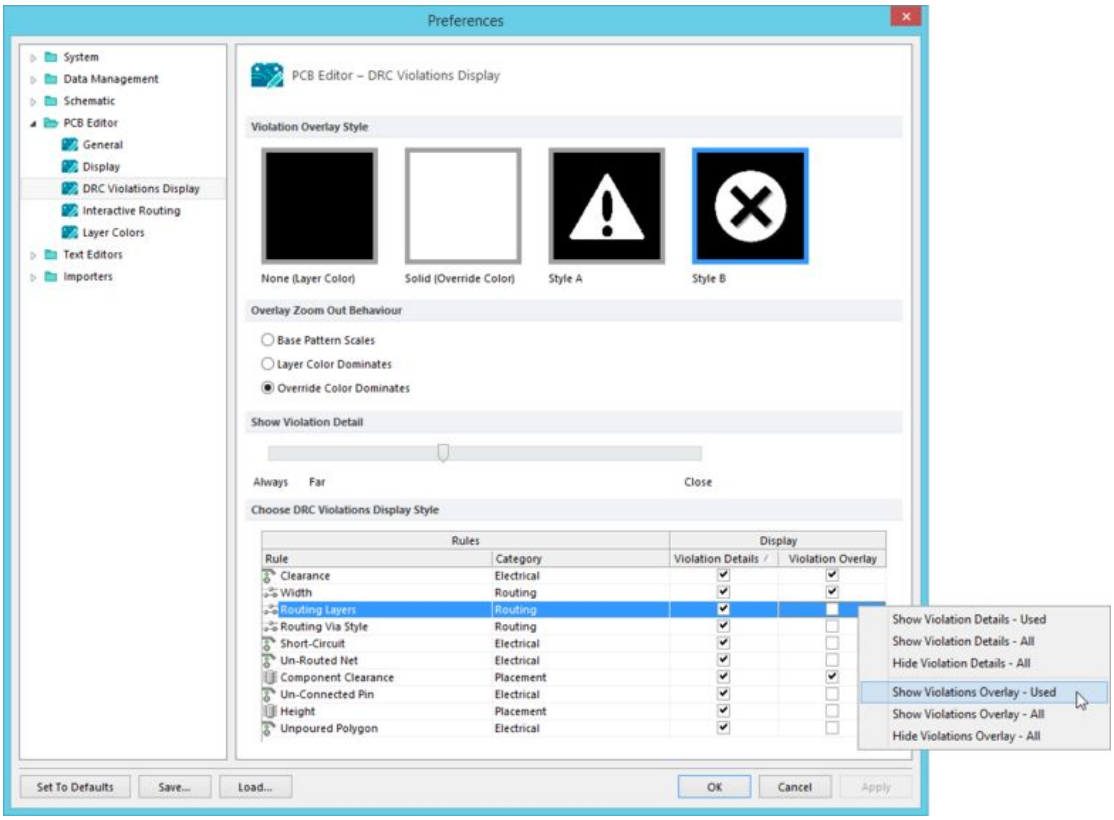
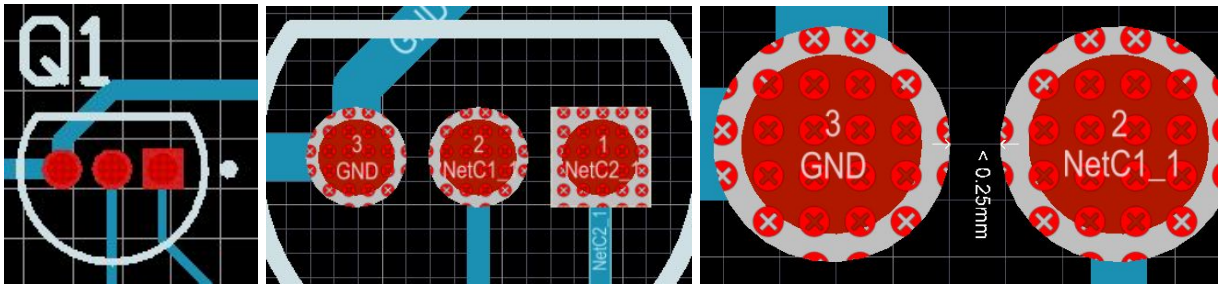
# Configuring the Display of Rule Violations

CircuitStudio has two techniques for displaying design rule violations, each with their own advantages. These are configured in the **PCB Editor - DRC Violations Display** page of the *Preferences* dialog:




- **Violation Overlay** - Violations are identified by the primitive-in-error being highlighted in the color chosen for the DRC Error Markers (configured in the *View Configurations* dialog). The default behavior is to show the primitives in a solid color when zoomed out, changing to the selected **Violation Overlay Style** as you zoom it. The default is **Style B**, a circle with a cross in it.
- **Violation Details** - As you zoom further in **Violation Detail** is added (if enabled), detailing the nature of the error. Use the **Show Violation Detail** slider to define at what zoom level the Violation Details start to display. Enable the required **Display** options in the *Preferences* dialog.




*Violations are shown in solid red (left image), as you zoom in this changes to an Overlay (center image), as you zoom in further Violation Details are added.*

# Preparing to run a Design Rule Check (DRC):

## Exercise

1. Access the View Configurations Dialog under the **Board Layers & Colors** Tab and ensure that the **Show** checkbox next to the **DRC Error Markers** option in the **System Colors** section is enabled (ticked) so that DRC error markers will be displayed.
    a. We also have a few errors related to Minimum Solder Mask, so while we are in here let's also turn on the Mask Layers
2. Confirm that the **Online DRC** (Design Rule Checking) system is enabled, the checkbox is in the **PCB Editor - General** page of the *Preferences* dialog. Keep the *Preferences* dialog open, and switch to the **PCB Editor - DRC Violations Display** page of the dialog.
3. The **PCB Editor - DRC Violations Display** page of the *Preferences* dialog is used to configure how violations are displayed in the workspace. There are 2 different methods available for displaying violations, each with their own strengths:
4. For the tutorial, right-click in the **Display** area of the **PCB Editor - DRC Violations Display** page of the *Preferences* dialog and select **Show Violation Details - Used**, then right-click again and select **Show Violation Overlay - Used**.
5. You are now ready to check the design for errors.

# Configuring the Rule Checker

The design is checked for violations by running the Design Rule Checker. Click the **Design Rule Check** button on the **Home** tab of the Ribbon to open the dialog. Both online and batch DRC are configured in this dialog.

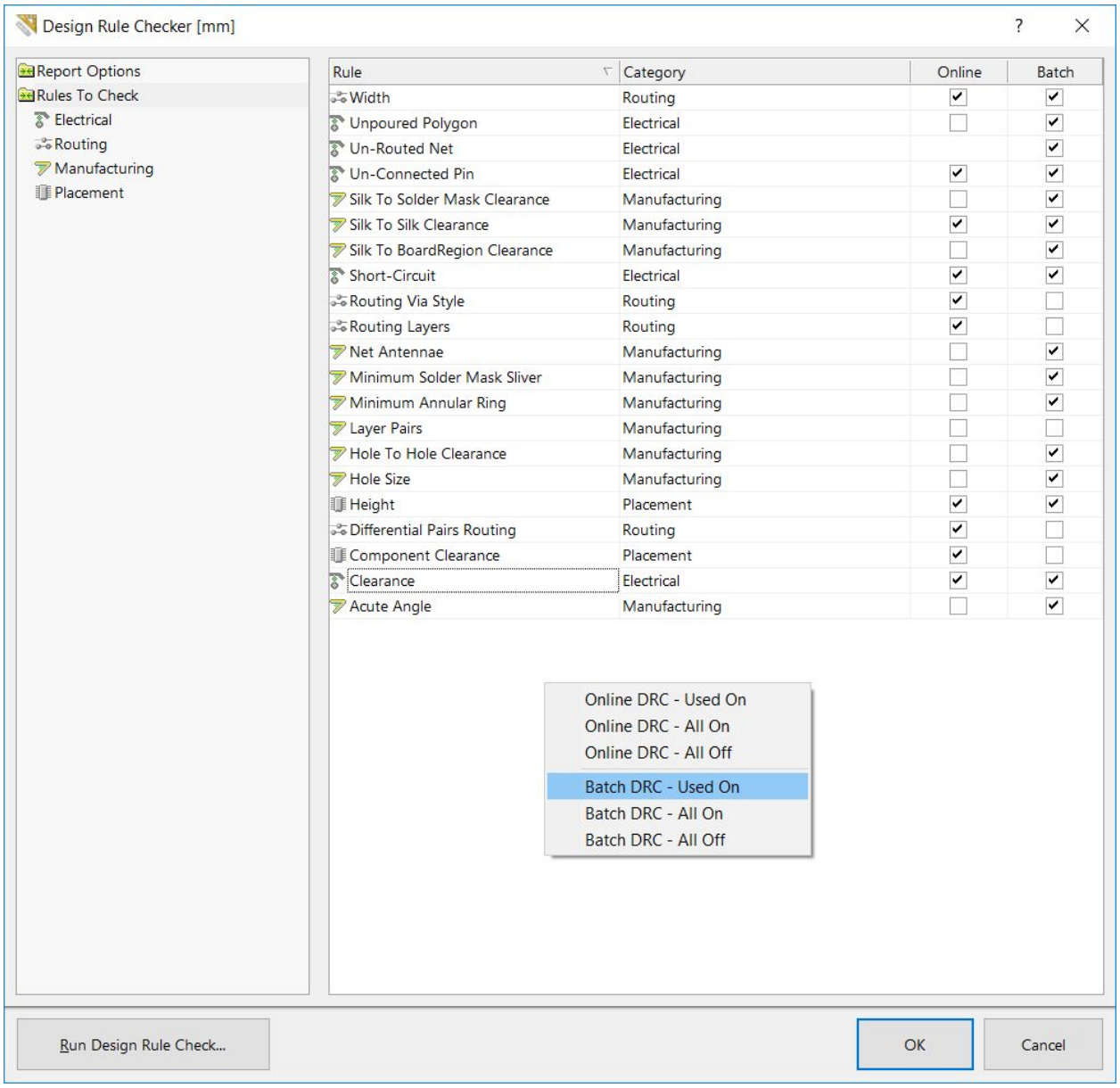

This section will not have defined Exercise steps, but you should be able to follow along with me, or read through the provided documentation to glean the steps you need to take from within the discussion.

## DRC Report Options

- By default, the dialog opens showing the **Report Options** page selected in the tree on the left of the dialog.
- The right side of the dialog displays a list of general reporting options. These options will be left at their defaults.

## DRC Rules to Check

- The testing of specific rules is configured in the **Rules to Check** section of the dialog, select this page in the tree on the left of the dialog to list all of the rule types (shown below). You can also examine them by type, for example **Electrical**, by selecting that page on the left of the dialog.
- For most rule types there are checkboxes for **Online** (check as you work) and **Batch** (check this rule when the **Run Design Rule Check** button is clicked).
- Click to enable/disable the rules as required. Alternatively, right-click to display the context menu. This menu allows you to quickly toggle the **Online** and **Batch** settings, we'll select the **Batch DRC - Used On** entry.




# Running a Design Rule Check (DRC)

When the **Run Design Rule Check** button at the bottom of the dialog is clicked, the DRC will run.

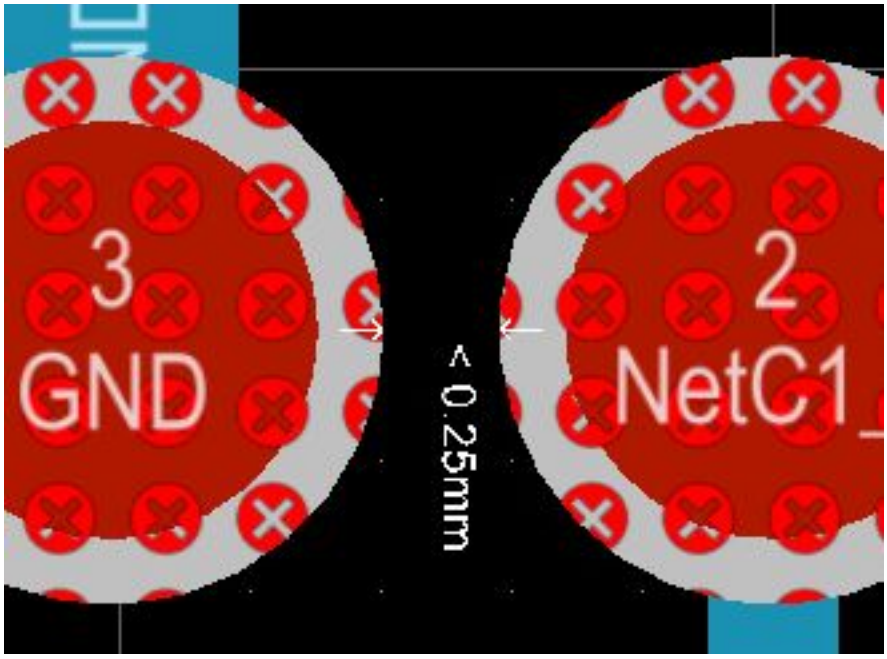
- The *Messages* panel will appear, listing all detected errors.
- If the Create Report File option was enabled in the Report Options page of the dialog, a **Design Rule Verification Report** will open in a separate document tab, the report for the tutorial is shown below.
- Below the summary of violating rules will be specific details about each violation.
- The links in the report are live, click on an error to jump back to the board and examine that error on the board. Note that the zoom level for this click action is configured in the **System**

- **General Settings** page of the *Preferences* dialog, experiment to find a zoom level that suits you.

## Identifying the Error Condition

When you are new to the software, a long list of violations can initially seem overwhelming. A good approach to managing this is to disable and enable rules in the *Design Rule Check* dialog, at different stages of the design process. It is not advisable to disable the design rules themselves, just the checking of them. For example, you would always disable the Un-Routed Net check until the board is fully routed.

- When a batch DRC is run on the tutorial board, there are 16 total violations - which means the measured values are less than the minimum amounts specified in the applicable design rule(s). You now know how to locate those violations (click the link in the report file, or double click in the *Messages* panel), and using the Violation Details, can understand the error condition.
- The image below shows the Violation Details for one of the clearance constraint errors, indicated by the white arrows and the 0.25mm text. The next step is to work out what the actual value is so you know how much it has failed by.




Apart from actually measuring the distance, there are two approaches to working out how much the rule has failed by, using either:

- the right-click **Violations** submenu, or
- the *PCB Rules and Violations* panel.

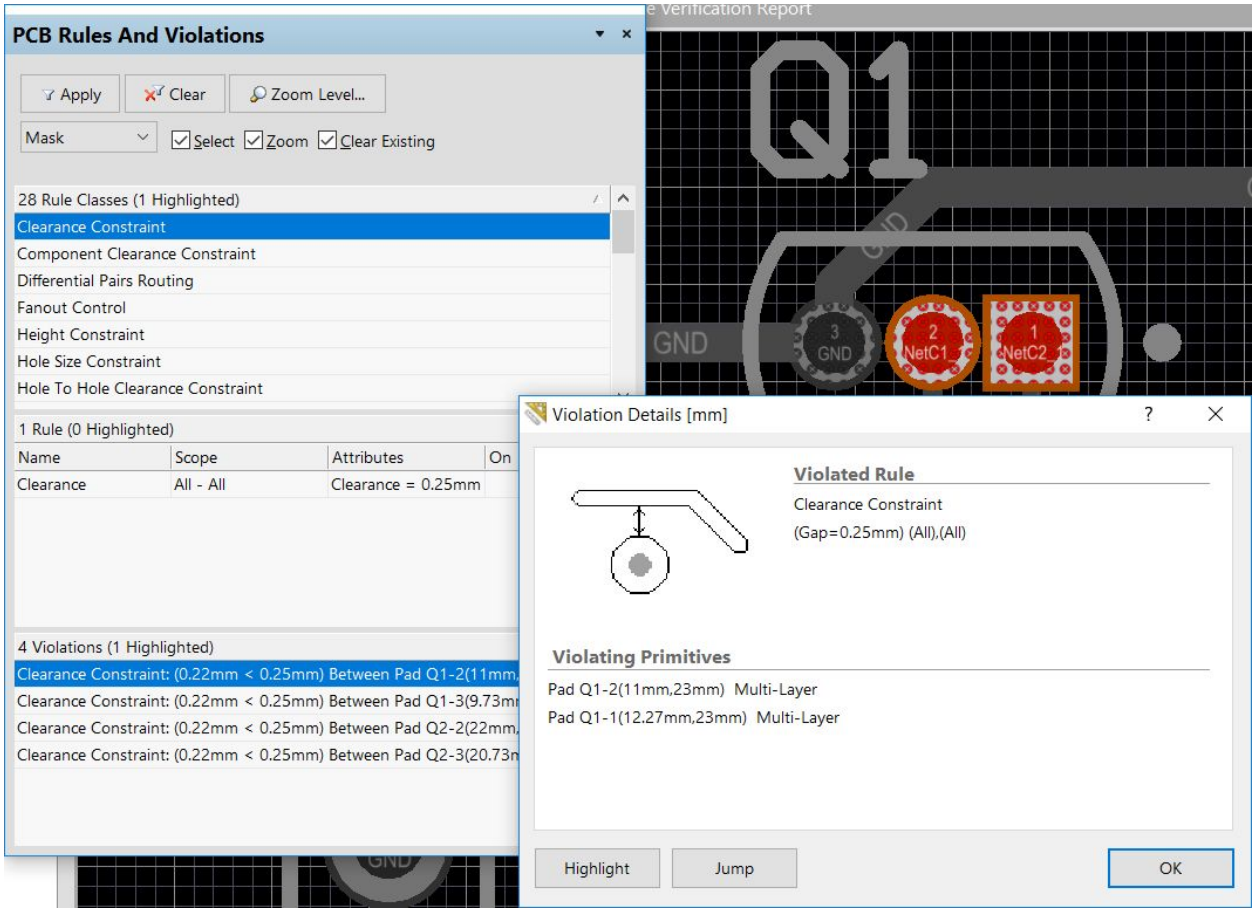
### The Violations Submenu

The right-click **Violations** submenu is accessed by right-clicking on an item marked with a Violation, and accessing Violations from the resulting Right Click menu

### The PCB Rules and Violations Panel

The second approach to understanding the error condition is to use the *PCB Rules and Violations* panel.

- Click the **View | PCB | Rules and Violations** button to display the panel.
- Click once on a Violation to jump to that violation, double-click on a violation to open the *Violation Details* dialog.




# Resolving the Violations

### Electrical Clearance

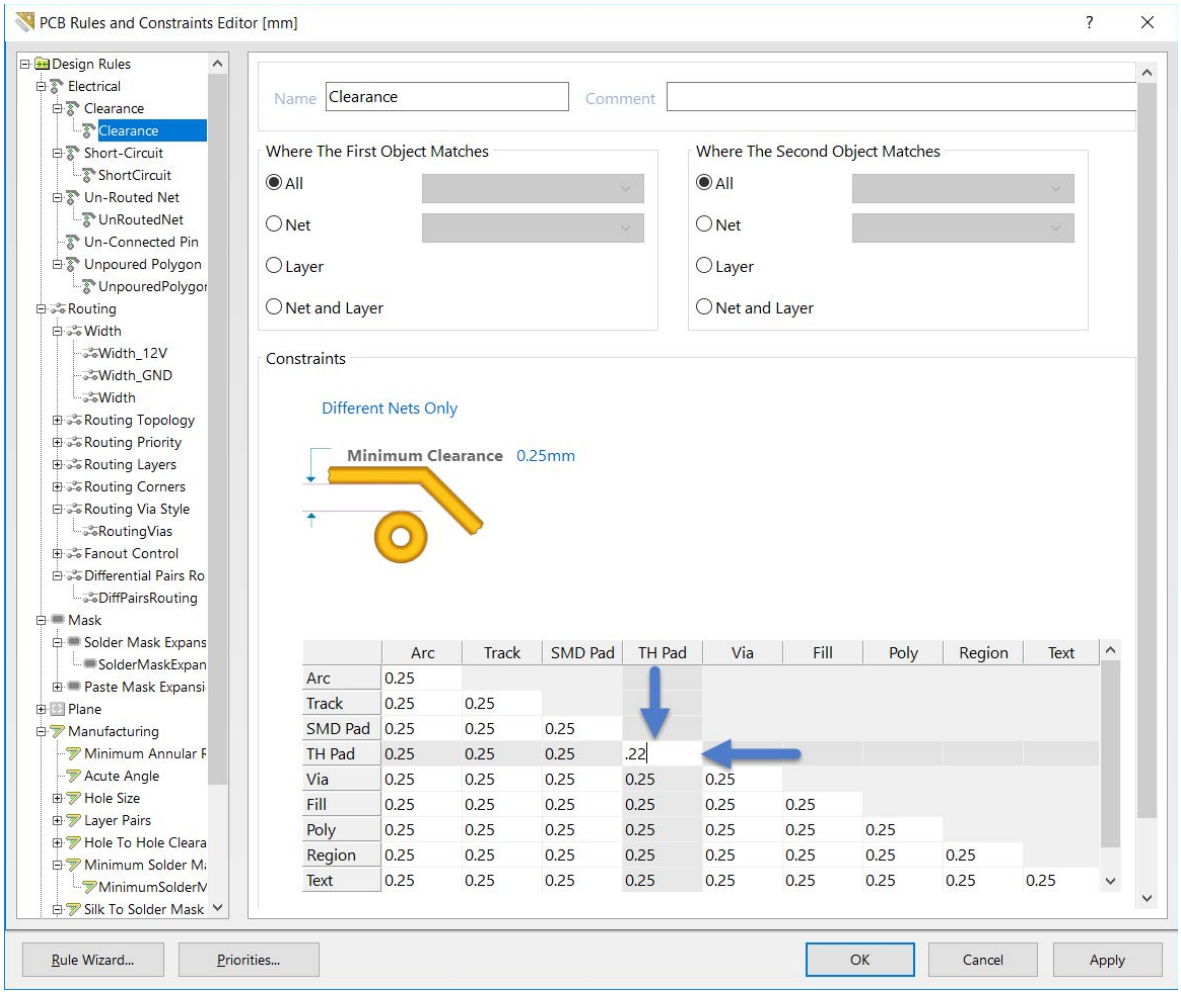
As with the previous section, there are no defined exercise steps here, but you will want to follow along with what I am doing, and complete these same steps in your design, either do this along with me, or watch the videos and retrace the steps within the

documentation provided with this video. There is a lot of show and tell here mixed in with a few changes we need to make, so to make it easier to read the exercise is not split out into its own section here.

As the designer you have to work out the most appropriate way of resolving each design rule violation. There are 2 ways of resolving the clearance constraint between the pads in Q1 and Q2:

- Decrease the size of the transistor footprint pads to increase the clearance between the pads, or
- Configure the rules to allow a smaller clearance between the transistor footprint pads.

Since the 0.25mm clearance is quite generous and the actual clearance is quite close to this value (0.22mm), a good choice in this situation would be to configure the rules to allow a smaller clearance. This can be done in the existing Clearance Constraint design rule - As a reminder, Design Rules are configured in the *PCB Rules and Constraints Editor* dialog (**Home Tab й Design Rules | Design Rules**)



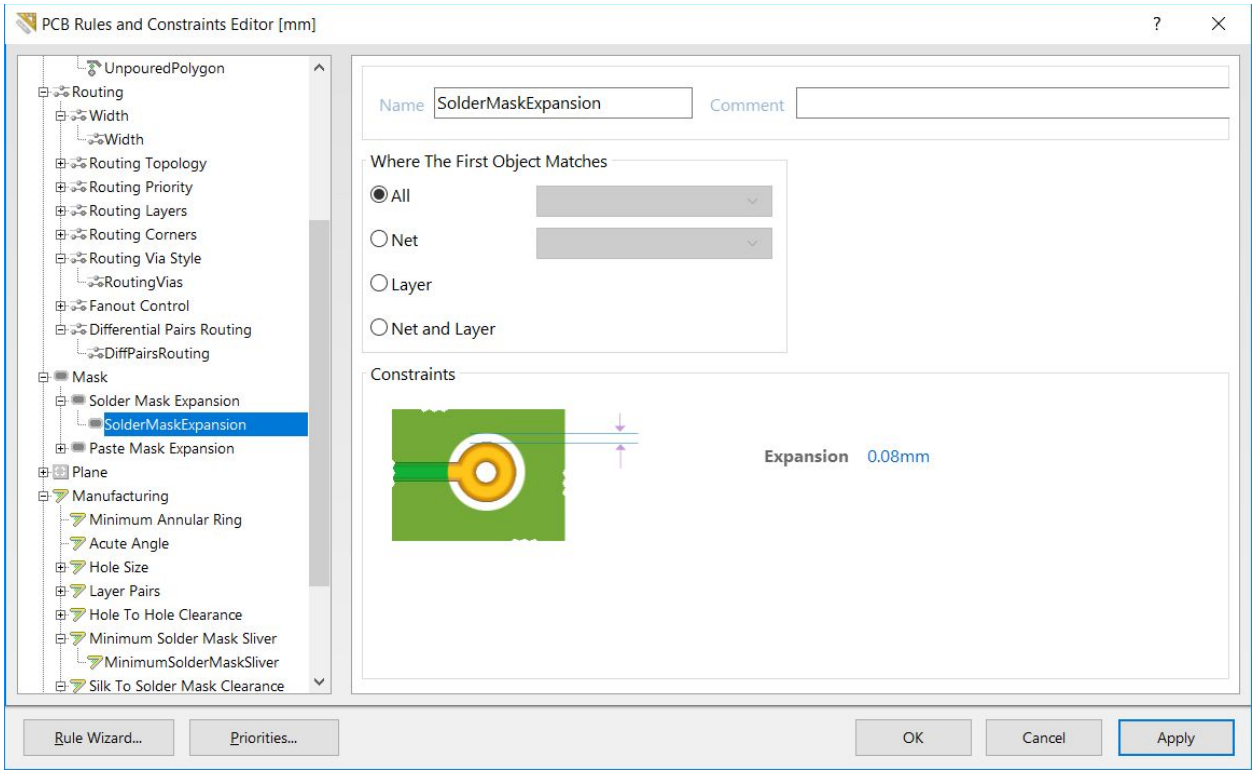
Change the TH Pad - to - TH Pad value to 0.22mm in the grid region of the rule constraint. To edit a cell first select it, then press **F2**.

This solution is acceptable in this situation because the only other component with thruhole pads is the connector, which has pads spaced over 1mm apart.

## Minimum Solder Mask Sliver

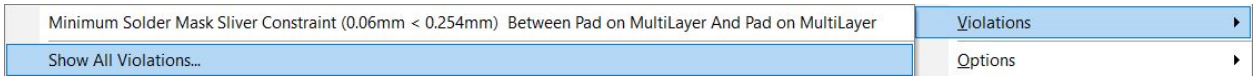
Next we need to look at the Minimum Solder Mask Sliver violations. To resolve these we can either adjust the Solder Mask Expansion rule to decrease the automatic Solder opening for your pads to be a smaller value, or we can adjust the Minimum Solder Mask Sliver value, or both. For this particular situation, let's make some minor modifications to both and enter some more sensible metric values into these rules.

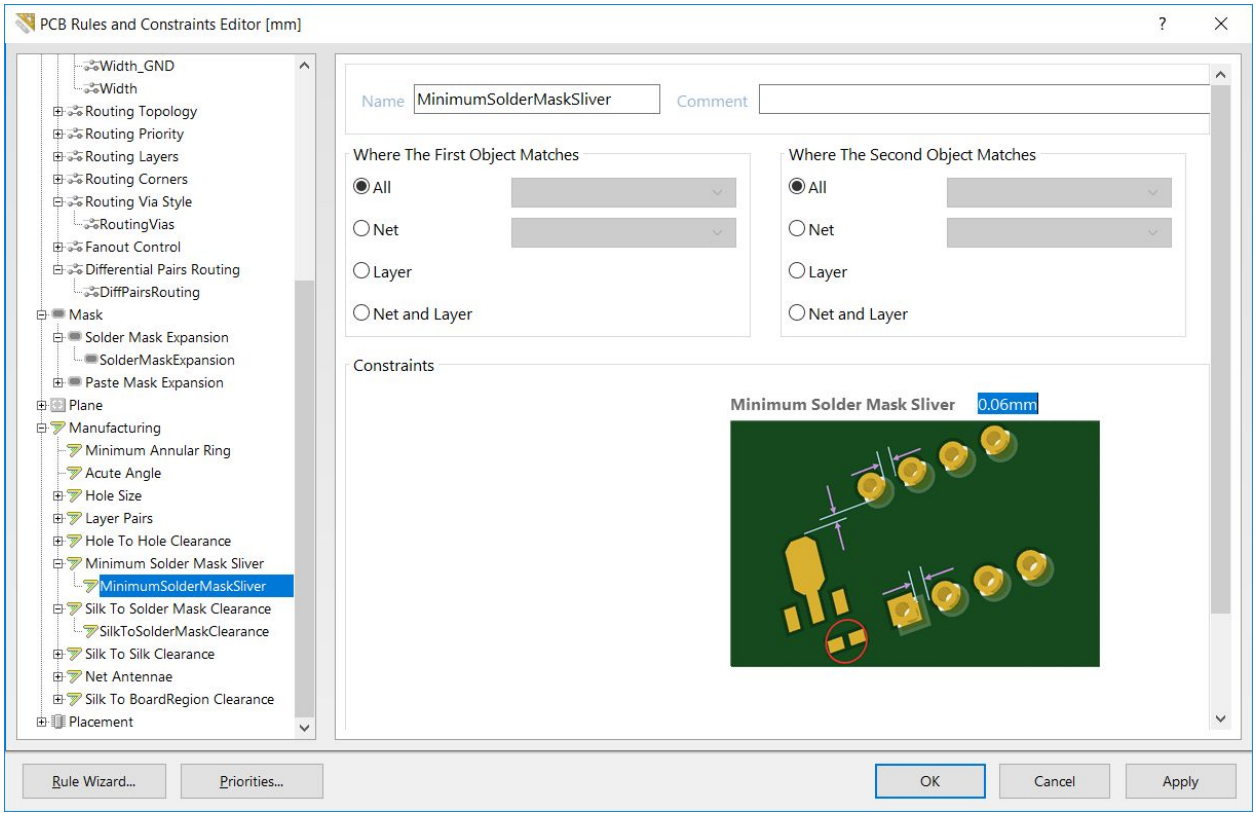
Open the Mask category within the Design Rules Editor, and select the Solder Mask Expansion rule, and change the value from .102mm to .08mm, this will reduce the solder opening for all component pads following the rule, which in turn will increase the width of the sliver created between two pads.




If we interrogate the Minimum Solder Mask Sliver violation after the expansion is changed, we will see it is still in violation, and that there is a sliver of the size .06mm, so we will change the Minimum Solder Mask Sliver to match this and clear the violation.

The values used here are not necessarily indicative of what is manufacturable, it is always best to check with your fab house to find out which values you should use to check your design for manufacturability concerns such as solder bridging. The default value of this rule is 10mil or .254mm and is likely larger than what we need.

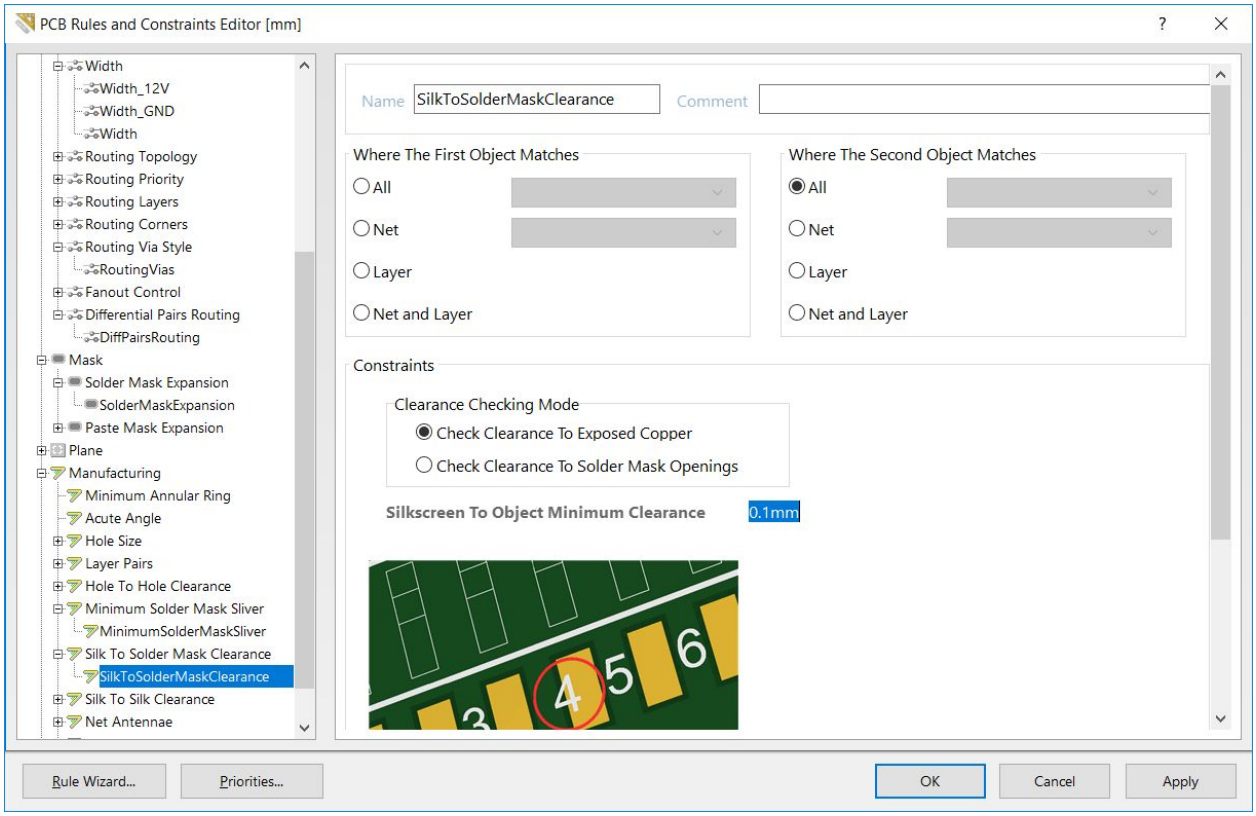



Change the Minimum Solder Mask Sliver rule to .06mm and rerun the Design Rule Check. With the changes we have made so far, we should only have some Silk to Soldermask Clearance violations left to review and resolve.

## Silk to Soldermask Clearance

Again, the default value for this rule is higher than we need, and in this particular case I just want to make sure my Silk is a short distance away from any Solder Mask openings, as I do not want Silkscreen being printed on top of my pad copper causing soldering issues, so we want a bit of space, but we really do not need too much.




Change the Silk to Soldermask Clearance rule from .254mm to .1mm click OK and then rerun the Design Rule Check.

We should now be Violation Free! **File** и **Save All** and we will continue on to generating our Outputs

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