



Estimating PSoC® Power Consumption

AN2216

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Associated Project: xls Spreadsheet

Associated Part Family: CY8C24xxx, CY8C27xxx, CY8C29xxx

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Software Version: PSoC Designer Version 4.1

Associated Application Notes: None

Abstract

Power consumption is a key issue for most applications. With an IC like the PSoC Mixed-Signal Array, where power consumption depends on a number of parameters used, power consumption estimation becomes very important. This Application Note explains the associated Microsoft Excel spreadsheet for power consumption in the CY8C24xxx, -27xxx, and -29xxx families of PSoC devices.

Introduction

The purpose of the associated spreadsheet is to estimate the power consumption of a PSoC device using different configurations. This Application Note describes how to use the spreadsheet to estimate power consumption for your PSoC project.

In general, enter the operating frequency or the number of the parameter selected. Data entry cells are yellow. Resultant current cells are green. If the value is out of range, the cell will turn red.

CPU Current

Enter CPU speed and PSoC supply voltage value in the corresponding cells. Estimated CPU current will appear in the corresponding green cell. Unused clock dividers (VC1, VC2, and VC3) should be set to the maximum value to minimize power.

Digital Block Current

Enter the input clock value for the digital blocks into the corresponding cells.

Row Current

For row current, enter the frequency values of the used output rows into the corresponding cells. Note that 12 MHz is the maximum clock speed for rows.

GPIO Current

To estimate GPIO current, two parameters are required. These are GPIO frequency and the number of GPIOs at the same frequency. GPIO frequency has the same 12 MHz limit as row frequency.

Analog Block Current

The analog block power level and op-amp bias level determine the current consumed by analog blocks. Enter the op-amp bias level and power level of the occupied analog blocks into the corresponding yellow cells. To minimize power consumption, utilize the lowest power level that still allows the analog block to meet system requirements at the specified column clock frequency.

Analog Output Buffer Current

Analog output buffer power consumption is effected by analog buffer power level. Select the analog output buffer power by writing '1' to the appropriate cell. To minimize power, use high power for the buffer only if the output frequency is greater than 50 kHz.

Reference Circuit Current

Reference power should be set greater than or equal to the power level of the highest power analog block occupied. If switched capacitor blocks are not used, the reference power can be safely set to "SC Off/Ref Low."

Conclusion

The total estimated current and total estimated power of the PSoC appears in the green cells at the bottom of the spreadsheet. The purpose of the spreadsheet is to help users estimate the power consumption of the CY8C24/27/29xxx device families. This estimate is based on testing a limited sample of PSoC devices and does not guarantee performance. External loads are not included in the estimate.

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