KEMET® TechTopics
...The Leading Edge

Vol. 5, No. 3 • Published by KEMET Electronics Corp. • P. O. Box 5928 • Greenville, S. C. 29606 • (803)963-6300 • June 1995

The sensitivity of multilayer ceramic capacitors to electrostatic discharges is an important subject which has probably not received adequate study. The following paper explores both the ESD "test" as it applies to capacitors and the results of capacitor testing.

KEMET would like to express its gratitude to co-author Phil (F.L.) Stair, Component Analyst/ESD Coordinator, Ford North Penn Electronics Facility, for his contributions of expertise and time in conducting many of the tests reported here.

Dr. John Piper
Vice President – Technology

ESD Withstand Capability of Multilayer Ceramic Capacitors (MLCs)

by J. Piper and J. D. Prymak, KEMET Electronics Corporation, and Phil (F.L.) Stair, Ford North Penn Electronics Facility

Awareness of electrostatic discharge (ESD) damage to electronic components has caused manufacturers to adopt various methods of determining the ESD threshold (sensitivity) of individual components. Some of these methods, designed for a broad range of components, subject capacitors to unrealistic stress levels not duplicated with other components and highly unlikely to be experienced in a "real world" application. In this article we will examine the causes of unrealistic conditions and the capabilities of MLCs to withstand ESD.

ESD Test and Testers

A current calibrated ESD simulator was incorporated in this investigation to apply voltage pulses to the capacitors under test. An Electro Tech Systems (ETS) Model 910 simulator was used with capability of positive and negative pulses applied at intervals between 0.5 seconds and 10 seconds. Peak voltage capability was 8,000 volts.

For this test, the standard condition for component evaluation was 5 positive pulses followed by 5 negative pulses. Capacitance, DF and IR were measured initially and post-test. Voltage levels were increased until a shift in post-test measurements was noted. Once a pre-determined shift selected by the customer was met, this voltage became the ESD threshold for that device.

The simulator is designed to duplicate the condition of a component being subjected to a sudden high-voltage discharge. We all experience uncomfortable ESD effects when we walk across a carpet in a dry atmosphere and then touch a conducting object, releasing the charge built up in our bodies. Under specific conditions, a spark may also be observed. It is this type of discharge, now standardized as the "Human Body Model," that causes much of the concern for the ESD susceptibility of electronic circuits. Our bodies act as a capacitor that builds up a charge until it can be discharged through a low impedance to ground.

The simulator can duplicate the "Human Body Model" as well as "Machine Models" (discharging from a mechanical source). The "Human Body Model" provides a 150 pFd charge capacitor discharged through a 1,500 ohms series resistance. The "Machine Model" has a 200 pFd charge capacitance and no series resistance.

To be charged, the capacitor is connected to a high-voltage power supply. The charge capacitor is then disconnected from the power supply and connected to the device under test. The charge is transferred to the device through any series resistance and usually dissipated through the resistance and the device.

Conservation of Charge

A capacitor presents an unusual situation for the ESD investigation. The charge in the charging capacitor is split between this capacitor and the capacitor under test (CUT). Ideally, the original charge,

$$Q_C = C_C \times V_T$$

where Cc is the capacitance of the charging capacitor and V_T is the voltage to which it was charged, is split between the two capacitors,

$$Q_C = (C_C + C_{CUT}) \times V_F$$

where C_{CUT} is the capacitance of the capacitor under test and V_F is the final voltage across each of the capacitors.

Multiple Pulses

ESD testing has adopted a common rule of testing: if a device must withstand any single experience, it should be tested to many of these experiences to establish capability. In this light, multiple ESD pulse exposures (both positive and negative) are often used to establish ESD capability. The problem with this multiple application with capacitors is that the capacitors store charge cumulatively. If no conditions are included to allow the capacitor to discharge between pulses, the cumulative charge results in higher voltages. If the cumulative ESD voltage is high enough with no discharge between pulses, it is only a matter of the capacitance and breakdown capability of the CUT, and the number of pulses attempted before the dielectric breakdown level is achieved and the capacitor fails. Many ESD simulators have programming capabilities for adjusting intervals between pulses as well as the number of pulses; and in the same standard offerings, make no provisions for discharge of the device under test, between pulses.

Table I shows the voltage developed across an ideal capacitor subjected to multiple 8 KV pulses from an ESD simulator with the "Human Body Model" discharge network. The series resistance is insignificant in this calculation due to charge transfer, and the assumption is that no charge is lost between pulses due to the extremely high insulation resistance of these devices.

The range of values for the table reflects the range of capacitance typical in a 50-volt rated X7R, 1206 style, surface mount chip capacitor. Note that these results were calculated for ideal capacitors and that the effect of the voltage coefficient of capacitance present in X7R or Y5V capacitors has not yet been considered.

Dielectric breakdown voltages (BDV) for MLCs are typically in the range of 500 to 1500 volts, which are readily exceeded with multiple pulses, especially in CUTs and low values of capacitance.

Bleeder Resistance

It was determined that a modification was necessary, in order to avoid charge accumulation during multiple pulse testing of the CUT. We have found that inserting a high value resistor in parallel with the CUT is a simple, but effective, way to achieve discharge. The resistance value selected had to provide a long RC time constant compared to the ESD pulse, but short compared to the pulse interval. We decided to use a 10 megohm resistor in our investigation.

Voltage Coefficient of Capacitance

As previously mentioned, the capacitance values in Table I are typical of X7R capacitors. However, the capacitance of X7R MLCs is highly dependent upon applied voltage as shown in Figure 1 (Note 1).

Capacitance vs. DC Bias for Typical X7R Capacitor

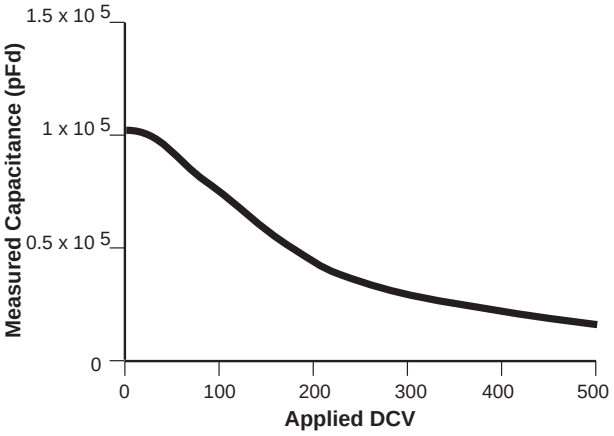

Figure 1. Capacitance vs DC Bias for Typical X7R Capacitor

Table I Voltage Build-Up - Ideal Capacitor

Capacitance (nfd)	Voltage Pulse 1	Voltage Pulse 2	Voltage Pulse 3	Voltage Pulse 4	Voltage Pulse 5	Voltage Pulse 8	Voltage Pulse 10	Voltage Pulse 15
100	12	24	36	48	60	95	119	178
33	36	72	108	144	179	285	355	526
10	118	235	349	463	574	898	1,107	1,601
3.3	348	681	999	1,303	1,594	2,394	2,871	3,893
1	1,043	1,951	2,740	3,426	4,023	5,385	6,023	7,017

Table II Voltage Build-Up - X7R Capacitors

Capacitance (nfd)	Voltage Pulse 1	Voltage Pulse 2	Voltage Pulse 3	Voltage Pulse 4	Voltage Pulse 5	Voltage Pulse 8	Voltage Pulse 10	Voltage Pulse 15
100	11	22	34	46	59	101	135	262
33	36	76	124	188	280	947	2,015	6,182
10	141	523	1,744	4,015	6,101	7,898	7,985	7,999
3.3	1,329	2,708	7,584	7,934	7.989	7,999	7,999	7,999
1	5,316	7,828	7,990	7,999	7,999	7,999	7,999	7,999

From Figure 1, it is readily seen that as the voltage on the capacitor increases, less capacitance is available to absorb the ESD charge. Now instead of the ideal relationship Q = C x V we must consider the voltage dependence of the capacitance and use the relationship:

$$Q = \int_{o}^{V} C(V)\,dV$$

Using the capacitance-voltage relationship from the measured data in Figure 1 and extrapolating the curve to higher voltages as necessary, then integrating, we obtain the charge retained by the CUT for any given voltage. As they are coupled, the resulting summary charge of the CUT and the charge capacitor can be calculated for all voltages through the ESD voltage. The following graph illustrates these combined and individual effects for a 10 nFd capacitor tested through 8 KV:

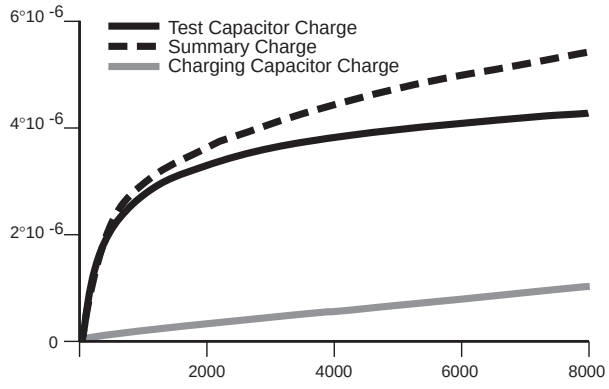

Figure 2. **Charge (Q) vs DC Bias**

Using the conservation of charge, the charge capacitor and CUT will combine to a summary charge after each pulse. We can deduce the voltage required for this pair to achieve the summary charge from Figure 2, and thus predict the voltage after each pulse.

Using the same inputs as used previously, Table I must be dramatically modified for typical X7R capacitors to the values in Table II.

Measured Voltages

The dramatic effect of considering the voltage coefficient of capacitance of the CUT was checked experimentally using a Keithley electrometer (Model 616). The electrometer had an input impedance of 2×10^{14} ohms shunted by 20 pF of capacitance. We estimate that the cable and connectors contribute another 10 pF of capacitance.

A 1.0 nF chip capacitor with a voltage coefficient of capacitance of -50% at 500V and a dielectric thickness of 2.4 mils was used. It was subjected to a 5 KV pulse from a 100 pF charging capacitor. Without the electrometer the calculated voltage after the pulse is 589V. With the extra 30 pFd of capacitance from the electrometer added to the CUT, the calculated number is 554V. We measured 540V; the calculated value assuming an ideal capacitor is 442V.

Another 1 nf X7R capacitor was tested, this time with a dielectric thickness of 1.4 mils and a voltage coefficient of capacitance of -70% at 500V. The predicted voltage without the electrometer in the circuit is 913V. With the electrometer the calculated voltage is 785V. Again, the ideal capacitor voltage calculation gives 442V. The measured value was 780V, in very good agreement with the model including the voltage coefficient effect.

Experimental Results

Approximately 1000 capacitors, either 0805 102 X7R or 1206 103 X7R values, were ESD tested. The test techniques used either the "human model" with a 150 pF charging capacitor and a 1500 ohm series resistor or the "machine model" with a 200 pF charging capacitor and no series resistor. Between 1 and 5 pulses were applied. Different tests were conducted with and without bleed resistor of 10 megohms in parallel with the capacitor under test. Some tests were conducted without a resistor, but with the capacitor shorted between pulses.

In early experiments we observed an occasional air discharge around the capacitor after the second or third of multiple ESD pulses, indicating that the capacitor had charged to a very high voltage. This led to exploration of the effect of physically discharging the test capacitor between pulses and the observation that the failure rate was greatly reduced when charge accumulation was avoided. Figure 3, therefore, presents the failure rate data in a matrix of the applied ESD pulse voltage and the maximum voltage derived from the accumulated charge as discussed earlier. Cells in which 10 or more capacitors were tested are shown on the chart. A failure was defined as a capacitor not meeting initial insulation resistance criteria. Figure 4 shows the failure rate versus estimated cumulative voltage as a result of 2000 volt pulses. These capa-citors have an ultimate breakdown voltage (i.e.,under a slow voltage ramp) of about 1000 volts.

The test results did not show a significant difference in failure rate between the machine model (no series resistance) and the human model (1500 ohm series resistance), so results for the two sets of tests were

combined to obtain Figures 3 and 4. In Figure 4 the 1900- and 2000-volt results came from human model tests; the 1960-volt result came from the machine model.

We were also unable to distinguish between the performance of 103-value capacitors and 102-value parts when compared on the basis of the same cumulative voltage. Obviously, under same test conditions the 103-value parts attained lower cumulative voltages, and so only a very few failures occurred.

4Discussion

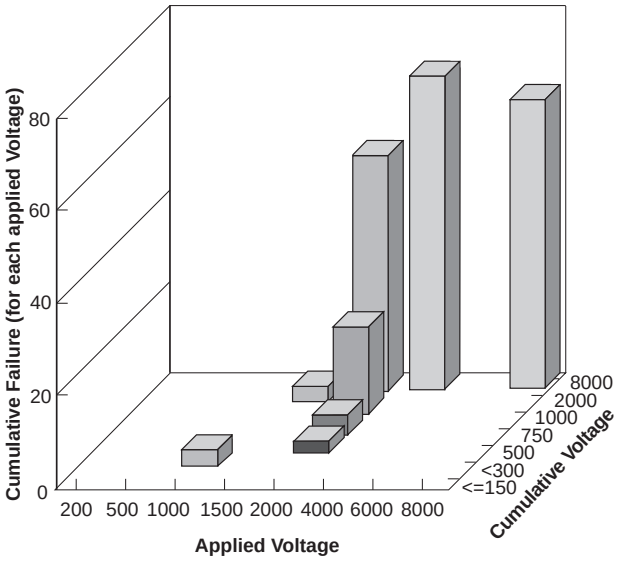

Figure 3.

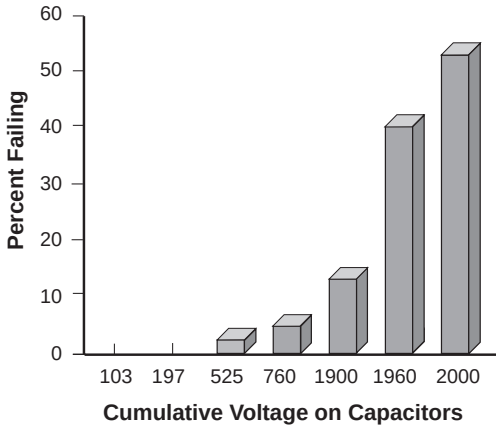

Figure 4.

The ESD tests, which were carried out in three groups at two laboratories, were designed simply to gauge ESD sensitivity and not focus on specific potential correlations. The strong relationship between failure rate and cumulative voltage on the capacitor quickly became evident. The importance of including the voltage coefficient of capacitance in estimating cumulative voltage was also shown.

The major weakness in this work is the identification of "failure." We use the common definition of a decrease in insulation resistance. Parts we considered "good" were not evaluated for degradation of parameters such as load humidity test performance or thermal shock sensitivity, which may have been compromised by the rapid application of a high voltage.

Published data on piezoelectric properties of barium titanate ceramics [3,4] predict that stresses of the order of the bulk modulus of rupture are generated with about 12V/um voltage stress or about 300-400 volts on capacitors of the design used here. An influence of charging rate on breakdown voltage values of MLCs has also been noted.[5]

The results here and the cited publications suggest caution when exposing MLCs to voltages high compared to their rating from any source.

Note 1.

Y5V characteristic capacitors typically have a much greater voltage dependence of capacitance than X7R capacitors[2]; however, the use of Y5V dielectrics is usually restricted to high capacitance value parts.

References

1. IEC 801-2, International Electrotechnical Commission, 1991.
2. KEMET Tech Topics 4, No. 1, February 1994.
3. Yoshikawa S. et al. "Multilayer Piezoelectric Actuators - Structures and Reliability", Collection of Technical Papers - AIAA/ASME Structures, Structural Dynamics and Materials Conference, 1991.
4. Boser, Otmar "Electromechanical Resonances in Ceramic Capacitors and Evaluation of Piezoelectric Materials' Properties," *Advanced Ceramic Materials* 2, 167, 1987.
5. Mandai, H., et al, "An Experimental Analysis of Ceramic Capacitor Voltage Breakdown," 3rd European Capacitor and Resistor Technology Symposium, CARTS-EUROPE, 1989.

© KEMET Electronics Corporation 1995