The most common LCD Module Interface Protocols are:
1. Parallel Interface
2. Serial Interface
3. Serial or Parallel Configuration to Microprocessor
4. TFT Interface

1. Parallel Interface
The parallel interface typically controls the LCD via 8 data pins and 3 control lines. The control lines used are Enable (E), Register Select (RS), and Read/Write (R/W). RS tells the LCD module if the information being sent is an Instruction or Data. The Enable tells the LCD module that the data or instruction in the register is ready to be interpreted by the LCD Module. Some controllers may have more than one Enable Control Line. The Read/Write tells the module whether to write data or read data from the register.

Types
*6800 type - Parallel Data(4-bit/8-bit), with Read/Write Line, Enable Line
*8080 type - Parallel Data(4-bit/8-bit) with Write Line, Read Line

Some parallel interface connection examples are:
a. 6800 8-Bit Parallel

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Function</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vss</td>
<td>Power Supply(GND)</td>
<td></td>
</tr>
<tr>
<td>Vdd</td>
<td>Power Supply(+)</td>
<td></td>
</tr>
<tr>
<td>Vo</td>
<td>Contrast Adjust</td>
<td></td>
</tr>
<tr>
<td>RS</td>
<td>Register Select Signal(L: Instruction H: Data)</td>
<td></td>
</tr>
<tr>
<td>R/W</td>
<td>Data Read/Write(L: Data Write H: Data Read)</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>Enable Signal</td>
<td></td>
</tr>
<tr>
<td>D0</td>
<td>Data Line</td>
<td>8 Bit Parallel Data Lines</td>
</tr>
<tr>
<td>D1</td>
<td>Data Line</td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td>Data Line</td>
<td></td>
</tr>
<tr>
<td>D3</td>
<td>Data Line</td>
<td></td>
</tr>
<tr>
<td>D4</td>
<td>Data Line</td>
<td></td>
</tr>
<tr>
<td>D5</td>
<td>Data Line</td>
<td></td>
</tr>
<tr>
<td>D6</td>
<td>Data Line</td>
<td></td>
</tr>
<tr>
<td>D7</td>
<td>Data Line</td>
<td></td>
</tr>
</tbody>
</table>
2. Serial Interface

Types

*Serial - Serial Data In, Register Select, Reset, and Serial Clock
Custom - Various configurations - Add Latch, Chip Select

*SPI (Serial Peripheral Interface)
SPI (3 wire) uses Serial Data Out, Serial Data In, and Serial Clock
SPI (4 wire) adds Chip Select
Custom - Various configurations - Serial Data, Serial Clock, Latch, Chip Select
Timing and operation may differ from usual SPI

*I²C (Inter-Integrated Circuit) - Uses Serial Data Line and Serial Clock

Some serial interface connection examples are:

Serial
Serial LCD controllers typically have one Serial Data Line that writes data and cannot read. Normally, a Register Select Line (Sometimes designated A0) is used to tell the controller whether the incoming data is display information or a controller command

Serial interface example

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<tr>
<th>Symbol</th>
<th>Function</th>
<th>Remark</th>
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<tbody>
<tr>
<td>SCL, SCLK, SCK, or CLK</td>
<td>Serial Clock(output from master)</td>
<td>Control line</td>
</tr>
<tr>
<td>CS, CSn(n = chip selected, &quot;1, 2, etc&quot;)</td>
<td>Chip Select(L: Chip Selected, H: Unselected)</td>
<td>Control line</td>
</tr>
<tr>
<td>SDI, DI, SI, SDA</td>
<td>Serial Data In</td>
<td>Data Line</td>
</tr>
<tr>
<td>A0</td>
<td>Register Select(L: Instruction H: Data)</td>
<td></td>
</tr>
<tr>
<td>RES</td>
<td>Reset(L: Enable H: Disable)</td>
<td></td>
</tr>
</tbody>
</table>

When RES is enabled, the register settings are initialized or cleared.
SPI Interface

SPI, or Serial Peripheral Interface bus, is a synchronous (data is synchronized to the clock) serial data link standard that operates in full duplex mode, which means that devices that can communicate with one another simultaneously. To do this, two data lines are required. With this standard, devices communicate in a master/slave mode, where the master device (host processor) initiates the data and the clock. The LCD module is the (or one of the) peripheral slave device(s) attached to the data bus. Multiple peripherals (display modules and other devices) are addressed on the same serial data bus. However, the LCD module will only listen to the data it sees when the Chip Select line is active (usually low). If the Chip Select line is inactive (usually High), the LCD module listens to the data on the bus, but ignores it. The SDO line is not active when this state occurs. The SPI bus is comprised of four logic signals, two control lines and two data lines and is commonly referred to as SPI (4 wire).

Serial SPI interface example

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<td>Control line</td>
</tr>
<tr>
<td>SDI, DI, SI</td>
<td>Serial Data In</td>
<td>Data Line</td>
</tr>
<tr>
<td>SDO, DO, SO</td>
<td>Serial Data Out</td>
<td>Data Line</td>
</tr>
</tbody>
</table>

Occasionally, SDI (serial data in) may be called out as MOSI (Master Out Slave In) from Motorola's original name for these lines and MISO (Master In Slave Out) for SDO. The chip select line may be alternatively labeled SS (Slave-Select), or STE (Slave Transmit Enable). SPI is sometimes referred to as National Semiconductor's trademark Microwire, which is essentially a predecessor of SPI, which only supports half duplex.

With CS (Chip-Select) the corresponding peripheral device is selected by the LCD Controller. This pin is mostly active-low. In the unselected state the SDO lines are hi-impedance and therefore inactive. The clock line SCL is brought to the device whether it is selected or not. The clock serves as synchronization of the data communication.

The chip select signal CS is optional for a single device system, because you could tie the CS input at the LCD Module low, if the other lines are dedicated to SPI use. This is sometimes called a 3 Wire SPI Interface.
SPI Data transmissions usually involve two shift registers. Most display module applications normally use 8-bit words. However, different size words, such as 12 bit, are also used. By convention, the most significant bit is shifted out of one shift register while the least significant bit is shifted in. The word is then written into memory if the CS (chip-select) is low (active). If not, the data is ignored.

Since the SPI interface protocol is a de facto standard, many variations of the standard protocol are used. For instance, chip manufacturers may use some of the parallel data lines when configuring the IC driver chip for serial communication. Chip manufacturers may use some of the parallel data lines when configuring the IC driver chip for serial communication.

I²C (Inter-Integrated Circuit)
I²C uses only two bi-directional lines, Serial Data Line (SDA) and Serial Clock (SCL), which are both typically pulled up with resistors. Typical voltages used are +5 V or +3.3 V. One of the strengths of the I²C interface is that a micro can control multiple devices with just the two I/O pins and software. Because of the I²C design, it is only half-duplex. The interface generally transmits 8-bit words, sending the most significant bit first.

3. Serial or Parallel Configuration to Microprocessor
Some modules may include additional control lines. Some examples are:
- C86 - Defines specific MPU interface. For instance, L: 8080, H: 6800,
- CS - Chip Select. For instance, L: Chip Selected, H: Chip Unselected
4. TFT Interface

Types
* 3 line, 4 line serial SPI
* 8 bits, 9 bits, 16 bits, 18 bits interface with 6800/8080 series MPU
* 6 bits, 8 bits serial RGB
* 16 bits, 18 bits, 24 bits parallel RGB
* 6 bits, 8 bits LVDS
* MIPI

Some TFT interface connection examples are:
3 line, 4 line serial SPI
8 bits, 9 bits, 16 bits, 18 bits interface with 6800/8080 series MPU
16 bits, 18 bits parallel RGB
24 bits parallel RGB
8 bits serial RGB
6 bits, 8 bits LVDS

(1) What is LVDS?
LVDS (Low Voltage Differential Signaling) technology provides a port with low voltage difference and differential signals. Developed by NS Technology Co., the American company uses digital video signal to resolve the excess amount of resource consumed and reducing EMI (Electromagnetic Interference) while transferring high bit rate data using TTL (Transistor-Transistor Logic). LVDS ports are able to perform differential data transfer between PCB traces or balanced cables with a relatively low output voltage swing (350mV), allowing a transfer speed up to several hundred megabit per second with low voltage difference. As a result, low voltage swing and low current drive applications have led to dramatic reduction in resource consumption and noise.

(2) Port Output
a. 6 bit LVDS output port
Using single circuit for transfers, the port implements 6 bit data for each primary color signals, thus delivering 18 bit RGB data. This output is also known as the 18 bit or 18 bit LVDS port.

b. 6 bit two-way LVDS output port
Using two-path dual circuit transfers, the port implements 6 bit data for each primary color signals, delivering 18 bit for single and dual channel data, totaling 36 bit RGB data. This output is also known as the 36 bit or 36 bit LVDS port.

c. 8 bit single circuit LVDS output port
Using single circuit for transfers, the port implements 8 bit data for each primary color signals, delivering 24 bit RDB data. This output is also known as the 24 bit or 24 bit LVDS port.

d. 8 bit two-way LVDS output port
Using two-path dual circuit transfers, the port implements 8 bit data for each primary color signals, delivering 24 bit for single and dual channel data, totaling 48 bit RGB data. This output is also known as the 48 bit or 48 bit LVDS port.

(3) Port Feature
a. High speed transfer rate averaging 655Mbps
b. Low voltage, low power consumption, low EMI with 350mV voltage
swing
c. Anti-interference capability, differential signal transfers

*MIPI*

（1）MIPI Definition
Connector ports for devices such like cameras, displays, basebands, and RF interfaces are standardized under MIPI Alliance specifications. These specifications include design, manufacturing costs, structural complexity, power consumption and degree of EMI.

（2）MIPI Features
a. High transfer speed: 1Gbps/Lane, 4Gbps throughput
b. Low consumption: 200mV voltage swing, 200mV common mode voltage
c. Noise control
d. Reduced pin number for efficient PCB layout